Listing and amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Cancel claims 1-10;

11. (Currently amended) A system for generating an error signal based on an error encountered while processing a received signal which includes an image representative datastream containing data packets, comprising:

a forward error detecting and correcting decoder which generates a first error signal;

a means for deriving a synchronization signal ~~derived~~ from the received signal;

a transport processor ~~interconnected~~ connected via a bus to the forward error detecting and correcting decoder and the means for deriving a synchronization signal so as to receive the first error signal and the synchronization signal, the transport processor generating a second error signal in response to the first error signal and the synchronization signal, wherein the second error signal begins at an earlier time than an associated data packet, and wherein the second error signal ends at a later time than the associated data packet;

a transport bus for forwarding to subsequent processing stages the data packets after having been processed by the forward error detecting and correcting decoder and wherein the data packets are forwarded as a series of discrete spaced apart frames;

wherein the second error signal is forwarded via the transport bus simultaneously with the data packets associated with the second error signal, wherein the second error signal being adapted to indicate an error in a defective data packet by having a duration that spans the frame of the defective data packet.

Cancel claim 12.

Cancel claim 13.

Cancel claim 14.

15. (Currently amended) The system of claim ~~14~~ 11, wherein the second error signal assumes a logical low state when no error is present in a data packet.

16. (Currently amended) The system of claim ~~15~~ 11, wherein the forward error detecting and correcting decoder is a Reed-Solomon decoder.

17. (Previously presented) The system of claim 11 wherein the transport processor is implemented as a microprocessor.

Cancel claims 18-22.